

Common Anode Capable High Brightness LED Driver with High Frequency Dimming

Check for Samples: [LM3434](#)

FEATURES

- Operating Input Voltage Range of -9V to -30V w.r.t. LED Anode
- Control Inputs are Referenced to the LED Anode
- Output Current Greater than 6A
- Greater than 30kHz PWM Frequency Capable
- Negative Output Voltage Capability Allows LED Anode to be Tied Directly to Chassis for Maximum Heat Sink Efficiency
- No Output Capacitor Required
- Up to 1MHz Switching Frequency
- Low I_Q , 1mA Typical
- Soft Start
- Adaptive Programmable ON Time Allows for Constant Ripple Current
- 24-Pin WQFN Package

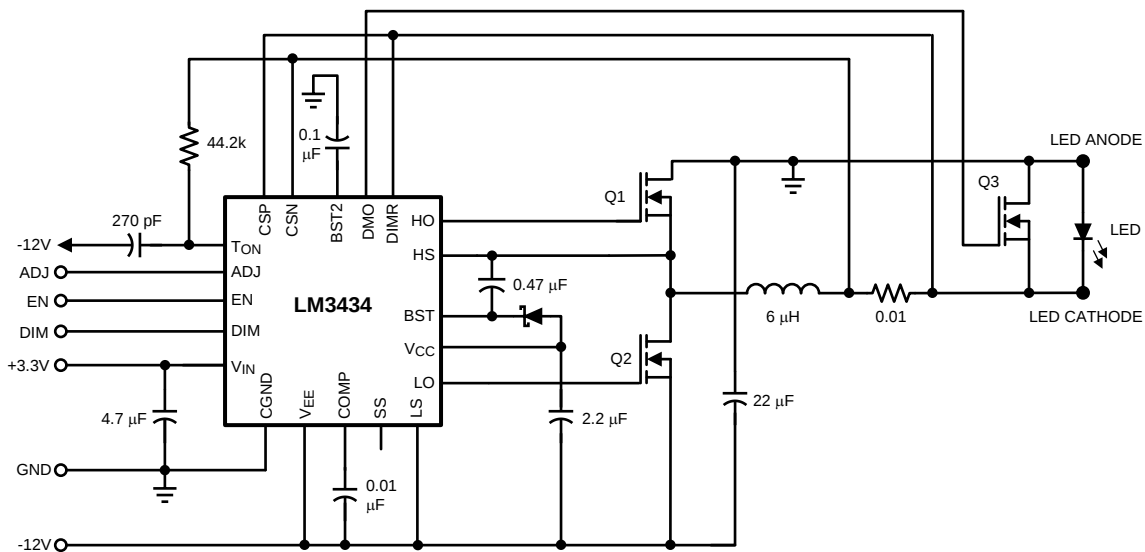
APPLICATIONS

- Projection Systems
- Solid State Lighting
- Automotive Lighting

DESCRIPTION

The LM3434 is an adaptive constant on-time DC/DC buck (step-down) constant current controller (a true current source). The LM3434 provides a constant current for illuminating high power LEDs. The output configuration allows the anodes of multiple LEDs to be tied directly to the ground referenced chassis for maximum heat sink efficacy. The high frequency capable architecture allows the use of small external passive components and no output capacitor while maintaining low LED ripple current. Two control inputs are used to modulate LED brightness. An analog current control input is provided so the LM3434 can be adjusted to compensate for LED manufacturing variations and/or color temperature correction. The other input is a logic level PWM control of LED current. The PWM functions by shorting out the LED with a parallel switch allowing high PWM dimming frequencies. High frequency PWM dimming allows digital color temperature control, interference blanking, field sequential illumination, and brightness control. Additional features include thermal shutdown, V_{CC} under-voltage lockout, and logic level shutdown mode. The LM3434 is available in a low profile 24-pin WQFN package.

TYPICAL APPLICATION CIRCUIT



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

All trademarks are the property of their respective owners.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Copyright © 2010–2013, Texas Instruments Incorporated

CONNECTION DIAGRAM

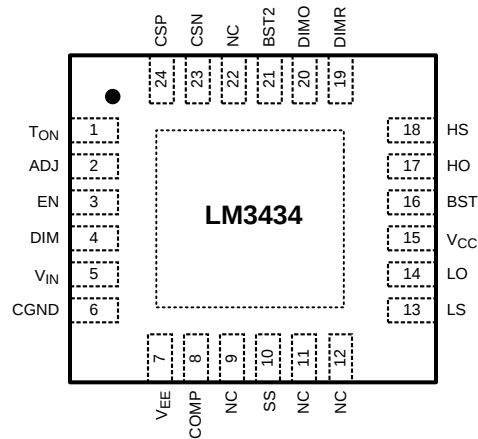


Figure 1. 24-Lead WQFN (Top View)
See RTW0024A Package

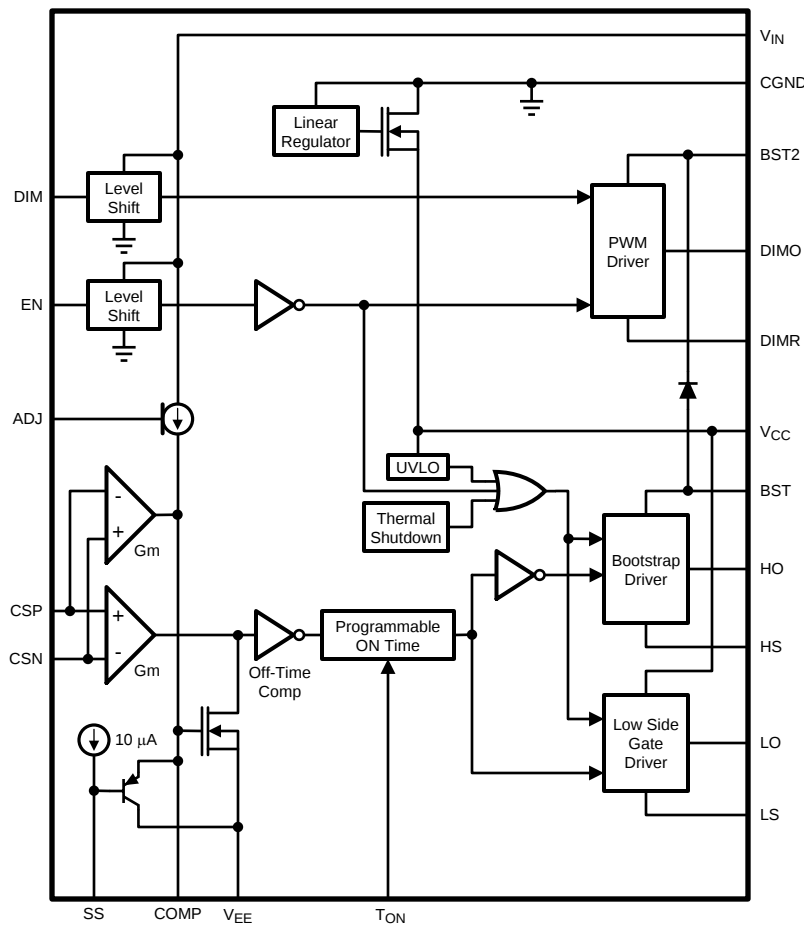
PIN DESCRIPTIONS

Pin	Name	Function
1	T _{ON}	On-time programming pin. Tie an external resistor (R _{ON}) from T _{ON} to CSN, and a capacitor (C _{ON}) from T _{ON} to V _{EE} . This sets the nominal operating frequency when the LED is fully illuminated.
2	ADJ	Analog LED current adjust. Tie to V _{IN} for fixed 60mV average current sense resistor voltage. Tie to an external reference to adjust the average current sense resistor voltage (programmed output current). Refer to the "V _{SENSE} vs. ADJ Voltage" graphs in the <i>Typical Performance Characteristics</i> section and the <i>Design Procedure</i> section of the datasheet.
3	EN	Enable pin. Connect this pin to logic level HI or V _{IN} for normal operation. Connect this pin to CGND for low current shutdown. EN is internally tied to V _{IN} through a 100k resistor.
4	DIM	Logic level input for LED PWM dimming. DIM is internally tied to CGND through a 100k resistor.
5	V _{IN}	Logic power input: Connect to positive voltage between +3.0V and +5.8V w.r.t. CGND.
6	CGND	Chassis ground connection.
7	V _{EE}	Negative voltage power input: Connect to voltage between –30V to –9V w.r.t. CGND.
8	COMP	Compensation pin. Connect a capacitor between this pin and V _{EE} .
9	NC	No internal connection. Tie to V _{EE} or leave open.
10	SS	Soft Start pin. Tie a capacitor from SS to V _{EE} to reduce input current ramp rate. Leave pin open if function is not used. The SS pin is pulled to V _{EE} when the device is not enabled.
11	NC	No internal connection. Tie to V _{EE} or leave open.
12	NC	No internal connection. Tie to V _{EE} or leave open.
13	LS	Low side FET gate drive return pin.
14	LO	Low side FET gate drive output. Low in shutdown.
15	V _{CC}	Low side FET gate drive power bypass connection and boost diode anode connection. Tie a 2.2μF capacitor between V _{CC} and V _{EE} .
16	BST	High side "synchronous" FET drive bootstrap rail.
17	HO	High side "synchronous" FET gate drive output. Pulled to HS in shutdown.
18	HS	Switching node and high side "synchronous" FET gate drive return.
19	DIMR	LED dimming FET gate drive return. Tie to LED cathode. If PWM dimming is not used this pin may be left open.
20	DIMO	LED dimming FET gate drive output. DIMO is a driver that switches between DIMR and BST2. If PWM dimming is not used this pin may be left open.
21	BST2	DIMO high side drive supply pin. Tie a 0.1μF between BST2 and CGND.
22	NC	No internal connection. Tie to V _{EE} or leave open.

PIN DESCRIPTIONS (continued)

Pin	Name	Function
23	CSN	Current sense amplifier inverting input. Connect to current sense resistor negative terminal.
24	CSP	Current sense amplifier non-inverting input. Connect to current sense resistor positive terminal.
EP	V _{EE}	Exposed Pad on the underside of the device. Connect this pad to a PC board plane connected to V _{EE} .

BLOCK DIAGRAM





These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS ⁽¹⁾

If Military/Aerospace specified devices are required, contact the Texas Instruments Semiconductor Sales Office/ Distributors for availability and specifications.

	VALUE / UNIT
V_{IN} , EN, DIM, ADJ to CGND	-0.3V to +7V
COMP, SS to V_{EE}	-0.3V to +7V
BST to HS	-0.3V to +7V
V_{CC} to V_{EE}	-0.3V to +7.5V
CGND, DIMR, CSP, CSN, T_{ON} to V_{EE}	-0.3V to +33V
HS to V_{EE} ⁽²⁾	-0.3V to +33V
LS to V_{EE}	-0.3V to +0.3V
HO output	HS-0.3V to BST+0.3V
DIMO to DIMR	-0.3V to +7V
LO output	LS-0.3V to V_{CC} +0.3V
BST2 to V_{EE}	-0.3V to 40V
Maximum Junction Temperature	150°C
Power Dissipation ⁽³⁾	Internally Limited
ESD Susceptibility Human Body Model ⁽⁴⁾	2kV

- (1) Absolute maximum ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions for which the device is intended to be functional, but device parameter specifications may **not be** ensured. For ensured specifications and test conditions, see the Electrical Characteristics.
- (2) The HS pin can go to -6V with respect to V_{EE} for 30ns and +22V with respect to V_{EE} for 50ns without sustaining damage.
- (3) The maximum allowable power dissipation is a function of the maximum junction temperature, $T_J(\text{MAX})$, the junction-to-ambient thermal resistance, θ_{JA} , and the ambient temperature, T_A . The maximum allowable power dissipation at any ambient temperature is calculated using: $P_D(\text{MAX}) = (T_J(\text{MAX}) - T_A) / \theta_{JA}$. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage. Thermal shutdown engages at $T_J=175^\circ\text{C}$ (typ.) and disengages at $T_J=155^\circ\text{C}$ (typ.).
- (4) Human Body Model, applicable std. JESD22-A114-C.

RECOMMENDED OPERATING CONDITIONS

	VALUE / UNIT
Operating Junction Temperature Range ⁽¹⁾	-40°C to +125°C
Storage Temperature	-65°C to +150°C
Input Voltage V_{IN} w.r.t. CGND	3.0V to 5.8V
Input Voltage V_{EE} w.r.t. CGND	-9V to -30V
ADJ Input Voltage Range to CGND	0V to V_{IN}

- (1) All limits specified at room temperature (standard typeface) and at temperature extremes (bold typeface). All room temperature limits are 100% production tested. All limits at temperature extremes are ensured via correlation using standard Statistical Quality Control (SQC) methods. All limits are used to calculate Average Outgoing Quality Level (AOQL).

ELECTRICAL CHARACTERISTICS

Specifications in standard type face are for $T_J = 25^\circ\text{C}$ and those with **boldface type** apply over the full **Operating Temperature Range** ($T_J = -40^\circ\text{C}$ to $+125^\circ\text{C}$). Minimum and Maximum limits are specified through test, design, or statistical correlation. Typical values represent the most likely parametric norm at $T_J = +25^\circ\text{C}$, and are provided for reference purposes only. Unless otherwise stated the following conditions apply: $V_{EE} = -12.0\text{V}$ and $V_{IN} = +3.3\text{V}$ with respect to CGND.

Symbol	Parameter	Conditions	Min ⁽¹⁾	Typ ⁽²⁾	Max ⁽¹⁾	Units
SUPPLY CURRENT						
I _{IN} V _{EE}	V _{EE} Quiescent Current	EN = CGND		142	250	μA
		EN = V _{IN} , Not Switching		1.0		mA
I _{IN} V _{IN}	V _{IN} Quiescent Current	EN = V _{IN} , Not Switching		450		μA
		EN = CGND		35	71	
OUTPUT CURRENT CONTROL						
V _{CS}	Current sense target voltage; V _{CS} = V _{CSP} – V _{CSN}	V _{ADJ} = V _{IN}	57	60	63	mV
G _{ADJ}	I _{ADJ} Gain = (V _{ADJ} -CGND)/(V _{CNP} -V _{CSN})	V _{IN} = 3.3V, V _{ADJ} = 0.5V or 1.5V w.r.t. CGND	15	16.67	18	V/V
I _{CSN}	Isense Input Current	V _{ADJ} = 1V w.r.t. CGND		-50		μA
		V _{ADJ} = V _{IN}		10		
I _{CSP}	Isense Input Current	V _{ADJ} = V _{IN}		60		μA
		V _{ADJ} = 1V w.r.t. CGND		1		
G _m	CS to COMP Transconductance; G _m = I _{COMP} / (V _{CSP} – V _{CSN} - V _{ADJ} /16.67)		0.6	1.3	2.2	mS
ON TIME CONTROL						
T _{ONTH}	On time threshold	V _{Ton} - V _{EE} at terminate ON time event	230	287	334	mV
GATE DRIVE AND INTERNAL REGULATOR						
V _{CCOUT}	V _{CC} output regulation w.r.t. V _{EE}	I _{CC} = 0mA to 20mA	6.3	6.75	7.1	V
V _{CCILIM}	V _{CC} current limit	V _{CC} = V _{EE}		-110		mA
R _{OLH}	HO output low resistance	I = 50mA source		2		Ω
R _{OHH}	HO output high resistance	I = 50mA sink		3		
R _{OLL}	LO output low resistance	I = 50mA source		2		Ω
R _{OHL}	LO output high resistance	I = 50mA sink		3		
R _{OLP}	DIMO output low resistance	I = 5mA source		20		Ω
R _{OHP}	DIMO output high resistance	I = 5mA sink		30		
FUNCTIONAL CONTROL						
V _{INUVLO}	V _{IN} undervoltage lockout	With respect to CGND		1.4		V
V _{CCUVLO}	V _{CC} - V _{EE} undervoltage lockout thresholds	On Threshold	6.0	6.6	7.0	V
		Off threshold	4.9	5.4	5.8	
V _{EN}	Enable threshold, with respect to CGND	Device on w.r.t. CGND			1.6	V
		Device off w.r.t. CGND	0.6			
R _{EN}	Enable pin pullup resistor			100		kΩ
V _{DIM}	DIM logic input threshold	DIM rising threshold w.r.t. CGND			1.6	V
		DIM falling threshold w.r.t. CGND	0.6			
R _{DIM}	DIM pin pulldown resistor			100		kΩ
I _{ADJ}	ADJ pin current		-1.0		1.0	μA
I _{SS}	SS pin source current			10		μA
R _{SS}	SS pin pulldown resistance	EN = CGND		1.0		kΩ

- (1) All limits specified at room temperature (standard typeface) and at temperature extremes (bold typeface). All room temperature limits are 100% production tested. All limits at temperature extremes are ensured via correlation using standard Statistical Quality Control (SQC) methods. All limits are used to calculate Average Outgoing Quality Level (AOQL).
- (2) Typical numbers are at 25°C and represent the most likely norm.

ELECTRICAL CHARACTERISTICS (continued)

Specifications in standard type face are for $T_J = 25^\circ\text{C}$ and those with **boldface type** apply over the full **Operating Temperature Range** ($T_J = -40^\circ\text{C}$ to $+125^\circ\text{C}$). Minimum and Maximum limits are specified through test, design, or statistical correlation. Typical values represent the most likely parametric norm at $T_J = +25^\circ\text{C}$, and are provided for reference purposes only. Unless otherwise stated the following conditions apply: $V_{EE} = -12.0\text{V}$ and $V_{IN} = +3.3\text{V}$ with respect to CGND.

Symbol	Parameter	Conditions	Min ⁽¹⁾	Typ ⁽²⁾	Max ⁽¹⁾	Units
AC SPECIFICATIONS						
T _{DTD}	LO and HO dead time	LO falling to HO rising dead time		26		ns
		HO falling to LO rising dead time		28		
T _{PDIM}	DIM to DIMO propagation delay	DIM rising to DIMO rising delay		96	175	ns
		DIM falling to DIMO falling delay		40	160	
THERMAL SPECIFICATIONS						
T _{JLIM}	Junction temperature thermal limit			175		°C
T _{JLIM(hyst)}	Thermal limit hysteresis			20		°C
θ _{JA}	WQFN package thermal resistance	JEDEC 4 layer board		39		°C/W

TYPICAL PERFORMANCE CHARACTERISTICS

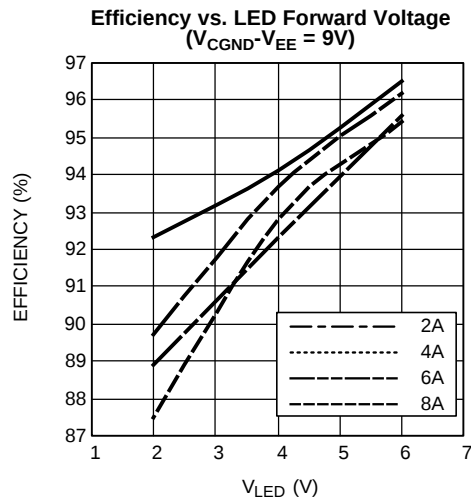


Figure 2.

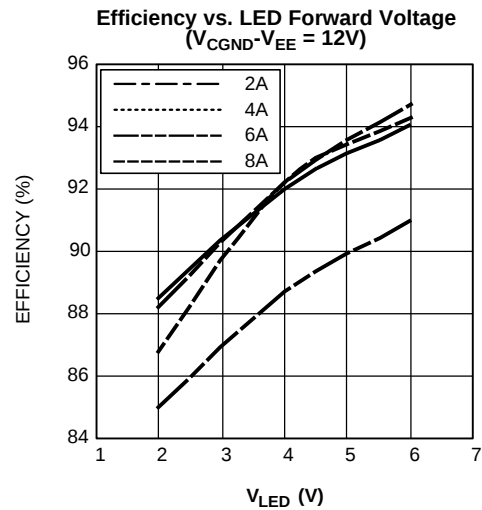


Figure 3.

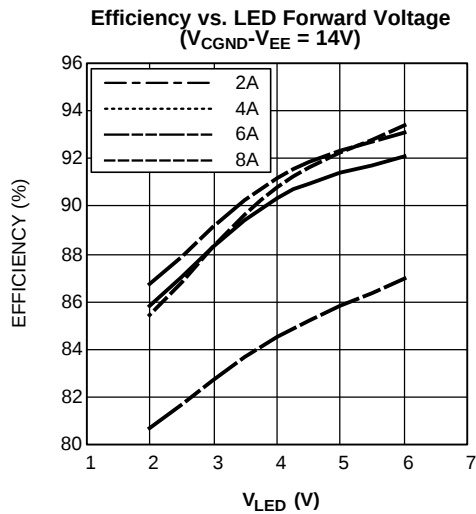


Figure 4.

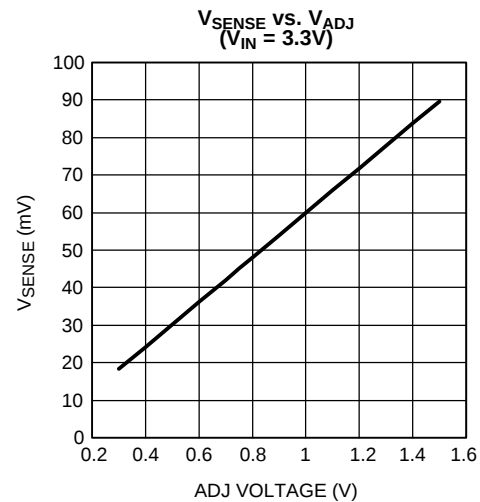


Figure 5.

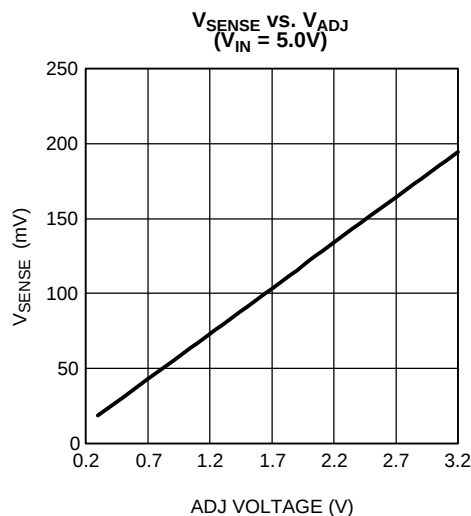


Figure 6.

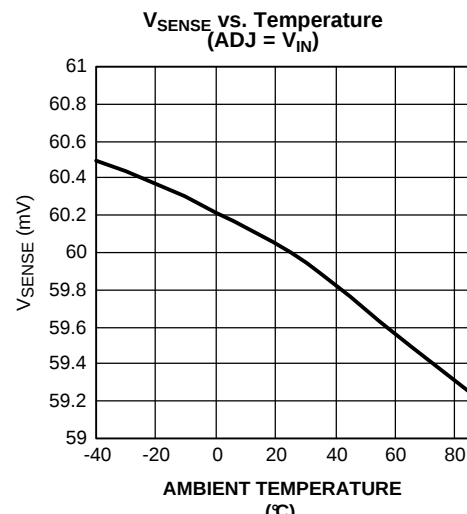


Figure 7.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

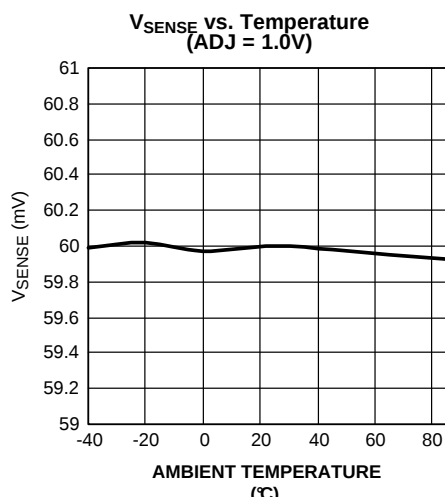


Figure 8.

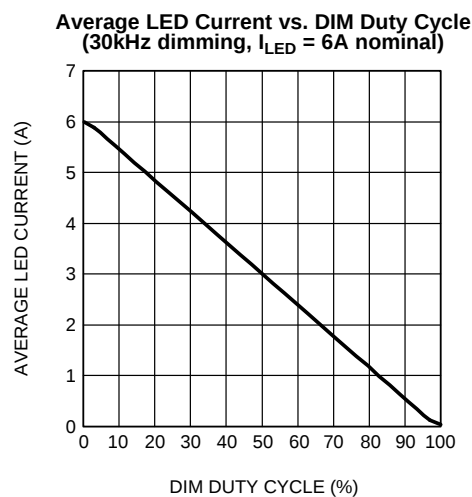
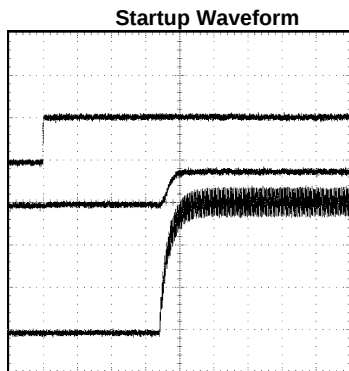
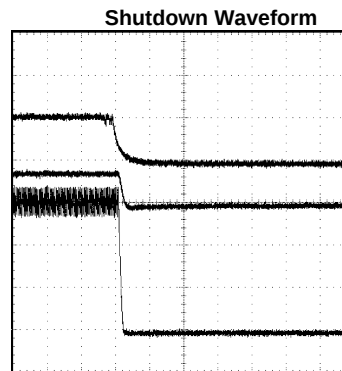


Figure 9.



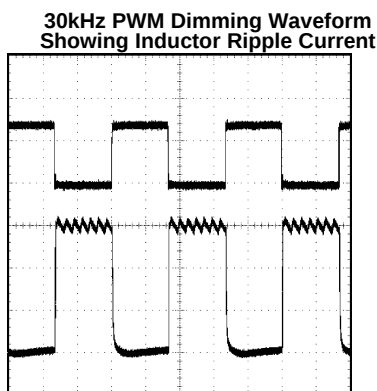
I_{LED} = 6A nominal, V_{IN} = 3.3V, V_{EE} = -12V, V_{LED} = 3V, SS = open
 Top trace: EN input, 2V/div, DC
 Middle trace: V_{EE} input current, 2A/div, DC
 Bottom trace: I_{LED}, 2A/div, DC
 T = 100μs/div

Figure 10.



I_{LED} = 6A nominal, V_{IN} = 3.3V, V_{EE} = -12V, V_{LED} = 3V, SS = open
 Top trace: EN input, 2V/div, DC
 Middle trace: V_{EE} input current, 2A/div, DC
 Bottom trace: I_{LED}, 2A/div, DC
 T = 100μs/div

Figure 11.



I_{LED} = 6A nominal, V_{IN} = 3.3V, V_{EE} = -12V
 Top trace: DIM input, 2V/div, DC
 Bottom trace: I_{LED}, 2A/div, DC
 T = 10μs/div

Figure 12.

OPERATION

CURRENT REGULATOR OPERATION

The LM3434 is a controller for a Continuous Conduction Buck Converter. Because of its buck topology and operation in the continuous mode, the output current is very well controlled. It only varies within a switching frequency cycle by the inductor ripple current. This ripple current is normally set at 10% of the DC current. Setting the ripple current lower than 10% is a useful tradeoff of inductor size for less LED light output ripple. Additional circuitry can be added to achieve any LED light ripple desired.

The LED current is set by the voltage across a sense resistor. This sense voltage is nominally 60mV but can be programmed higher or lower by an external control voltage.

The running frequency of the converter is programmed by an external RC network in conjunction with the LED's forward voltage. The frequency is nominally set around 200kHz to 500kHz. Fast PWM control is available by shorting the output of the current source by a MOSFET in parallel with the LED. During the LED OFF time the running frequency is determined by the RC network and the parasitic resistance of the output circuit including the DIM FET $R_{DS(on)}$.

The LM3434 system has been evaluated to be a very accurate, high compliance current source. This is manifest in its high output impedance and accurate current control. The current is measured to vary less than 6mA out of 6A when transitioning from LED OFF (output shorted) to LED ON (output ~6V).

PROTECTION

The LM3434 has dedicated protection circuitry running during normal operation. The thermal shutdown circuitry turns off all power devices when the die temperature reaches excessive levels. The V_{CC} undervoltage lockout (UVLO) comparator protects the power devices during power supply startup and shutdown to prevent operation at voltages less than the minimum operating input voltage. The V_{CC} pin is short circuit protected to V_{EE} . The LM3434 also features a shutdown mode which decreases the supply current to approximately 35µA.

The ADJ, EN, and DIM pins are capable of sustaining up to +/-2mA. If the voltages on these pins will exceed either V_{IN} or CGND by necessity or by a potential fault, an external resistor is recommended for protection. Size this resistor to limit pin current to under 2mA. A 10k resistor should be sufficient. This resistor may be used in any application for added protection without any impact on function or performance.

Output Open Circuit

The LM3434 can be powered up with an open circuit without sustaining any damage to the circuit. During normal operation the circuit will also tolerate an open circuit condition without sustaining damage provided a schottky diode is placed within the circuit to provide a current path to discharge the energy stored in the inductor. The anode of the schottky should be connected to the negative supply voltage while the cathode should be connected to the point where the inductor and sense resistor intersect. This diode should have a surge current rating equal to that of the maximum LED current driven.

DESIGN PROCEDURE

This section presents guidelines for selecting external components.

SETTING LED CURRENT CONTROL

LM3434 uses average current mode control to regulate the current delivered to the LED (I_{LED}). An external current sense resistor (R_{SENSE}) in series with the LED is used to convert I_{LED} into a voltage that is sensed by the LM3434 at the CSP and CSN pins. CSP and CSN are the inputs to an error amplifier with a programmed input offset voltage (V_{SENSE}). V_{SENSE} is used to regulate I_{LED} based on the following equation:

$$I_{LED} = V_{SENSE} / R_{SENSE} \quad (1)$$

FIXED LED CURRENT

The ADJ pin sets V_{SENSE} . Tie ADJ to V_{IN} to use a fixed 60mV internal reference for V_{SENSE} . Select R_{SENSE} to fix the LED current based on the following equation:

$$R_{SENSE} = 60\text{mV}/I_{LED} \quad (2)$$

ADJUSTABLE LED CURRENT

When tied to an external voltage the ADJ pin sets V_{SENSE} based on the following equation:

$$V_{SENSE} = (V_{ADJ} - V_{CGND})/16.6 \quad (3)$$

When the reference on ADJ is adjustable, V_{SENSE} and I_{LED} can be adjusted within the linear range of the ADJ pin. This range has the following limitations:

$$0.3\text{V} < V_{ADJ} < (\text{The greater of } 1.5\text{V} \text{ or } (V_{IN} - 1.9\text{V})) \quad (4)$$

When V_{ADJ} is less than this linear range the V_{SENSE} is specified by design to be less than or equal to $0.3\text{V}/16.667$. When V_{ADJ} is greater than this linear range and less than $V_{IN} - 1\text{V}$, V_{SENSE} is specified by design to be less than or equal to $V_{ADJ}/16.667$. If V_{ADJ} is greater than $V_{IN} - 1\text{V}$, V_{SENSE} switches to 60mV.

INPUT CAPACITOR SELECTION

A low ESR ceramic capacitor is needed to bypass the MOSFETs. This capacitor is connected between the drain of the synchronous FET (CGND) and the source of the main switch (V_{EE}). This capacitor prevents large voltage transients from appearing at the V_{EE} pin of the LM3434. Use a $22\mu\text{F}$ value minimum with X5R or X7R dielectric. In addition to the FET bypass capacitors, additional bypass capacitors should be placed near the V_{EE} and V_{IN} pins and should be returned to CGND.

The input capacitor must also be sized to handle the dimming frequency input ripple when the DIM function is used. This ripple may be as high as 85% of the nominal DC input current (at 50% duty cycle). When dimming this input capacitor should be selected to handle the input ripple current.

RECOMMENDED OPERATING FREQUENCY AND ON TIME "TIME_{ON}" CALCULATION

Although the switching frequency can be set over a wide range, the following equation describes the recommended frequency selection given inexpensive magnetic materials available today:

$$f = \frac{A}{\sqrt{I_{LED}}} \text{ (MHz)} \quad (5)$$

In the above equation $A=1.2$ for powdered iron core inductors and $A=0.9$ or less for ferrite core inductors. This difference takes into account the fact that ferrite cores generally become more lossy at higher frequencies. Given the switching frequency f calculated above, TIME_{ON} can be calculated. If V_{LED} is the forward voltage drop of the LED that is being driven, TIME_{ON} can be calculated with the following equation:

$$\text{TIME}_{ON} = \frac{V_{LED}}{f|V_{EE}|} \quad (6)$$

TIMING COMPONENTS (R_{ON} and C_{ON})

Using the calculated value for TIME_{ON} , the timing components R_{ON} and C_{ON} can be selected. C_{ON} should be large enough to dominate the parasitic capacitance of the T_{ON} pin. A good C_{ON} value for most applications is 1nF. Based on calculated TIME_{ON} , C_{ON} , and the nominal V_{EE} and V_{LED} voltages, R_{ON} can be calculated based on the following equation:

$$R_{ON} = \frac{\text{TIME}_{ON}}{C_{ON}(0.3/(|V_{EE}| - V_{LED}))} \quad (7)$$

INDUCTOR SELECTION

The most critical inductor parameters are inductance, current rating, and DC resistance. To calculate the inductance, use the desired peak to peak LED ripple current (I_{RIPPLE}), R_{ON} , and C_{ON} . A reasonable value for I_{RIPPLE} is 10% of I_{LED} . The inductor value is calculated using the following equation:

$$L = \frac{0.3 \times R_{\text{ON}} \times C_{\text{ON}}}{I_{\text{RIPPLE}}} \quad (8)$$

For all V_{LED} and V_{EE} voltages, I_{RIPPLE} remains constant and is only dependent on the passive external components R_{ON} , C_{ON} , and L .

The I^2R loss caused by the DC resistance of the inductor is an important parameter affecting the efficiency. Lower DC resistance inductors are larger. A good tradeoff point between the efficiency and the core size is letting the inductor I^2R loss equal 1% to 2% of the output power. The inductor should have a current rating greater than the peak current for the application. The peak current is I_{LED} plus $1/2 I_{\text{RIPPLE}}$.

POWER FET SELECTION

FETs should be chosen so that the $I^2R_{\text{DS(on)}}$ loss is less than 1% of the total output power. Analysis shows best efficiency with around $8\text{m}\Omega$ of $R_{\text{DS(on)}}$ and 15nC of gate charge for a 6A application. All of the switching loss is in the main switch FET. An additional important parameter for the synchronous FET is reverse recovery charge (Q_{RR}). High Q_{RR} adversely affects the transient voltages seen by the IC. A low Q_{RR} FET should be used.

DIM FET SELECTION

Choose a DIM FET with the lowest $R_{\text{DS(on)}}$ for maximum efficiency and low input current draw during the DIM cycle. The output voltage during DIM will determine the switching frequency. A lower output voltage results in a lower switching frequency. If the lower frequency during DIM must be bound, choose a FET with a higher $R_{\text{DS(on)}}$ to force the switching frequency higher during the DIM cycle.

Placement of the Parallel Dimming FET

When using a FET in parallel with the LED for PWM dimming special consideration must be used for the location of the FET. The ideal placement of the FET is *directly* next to the LED. Any distance between this FET and the LED results in line inductance. Fast current changes through this inductance can induce large voltage spikes due to $v = L di/dt$. These can be mitigated by either reducing the distance between the FET and the LED and/or slowing the PWM edges, and therefore the di/dt , by using some gate resistance on the FET. In cases where the dimming FET is not placed close to the LED and/or very fast switching edges are desired the induced voltages can become great enough to damage the dimming FET and/or the LM3434 HS pin. This can also result in a large spike of current into the LED when the FET is turned off. In these cases a snubber should be placed across the dimming FET to protect the device(s).

BOOTSTRAP CAPACITORS

The LM3434 uses two bootstrap capacitors and a bypass capacitor on V_{CC} to generate the voltages needed to drive the external FETs. A $2.2\mu\text{F}$ ceramic capacitor or larger is recommended between the V_{CC} and LS pins. A $0.47\mu\text{F}$ is recommended between the HS and BST pins. A $0.1\mu\text{F}$ is recommended between BST2 and CGND.

SOFT-START CAPACITOR

The LM3434 integrates circuitry that, when used in conjunction with the SS pin, will slow the current ramp on start-up. The SS pin is used to tailor the soft-start for a specific application. A capacitor value of $0.1\mu\text{F}$ on the SS pin will yield a 12mS soft start time. For most applications soft start is not needed.

ENABLE OPERATION

The EN pin of the LM3434 is designed so that it may be controlled using a 1.6V or higher logic signal. If the enable function is not used, the EN pin may be tied to V_{IN} or left open. This pin is pulled to V_{IN} internally through a 100k pull up resistor.

PWM DIM OPERATION

The DIM pin of the LM3434 is designed so that it may be controlled using a 1.6V or higher logic signal. The PWM frequency easily accommodates more than 40kHz dimming and can be much faster if needed. If the PWM DIM pin is not used, tie it to CGND or leave it open. The DIM pin is tied to CGND internally through a 100k pull down resistor.

LAYOUT CONSIDERATIONS

The LM3434 is a high performance current driver so attention to layout details is critical to obtain maximum performance. The most important PCB board design consideration is minimizing the loop comprised by the main FET, synchronous FET, and their associated decoupling capacitor(s). Place the V_{CC} bypass capacitor as near as possible to the LM3434. Place the PWM dimming/shunt FET as close to the LED as possible. A ground plane should be used for power distribution to the power FETs. Use a star ground between the LM3434 circuitry, the synchronous FET, and the decoupling capacitor(s). The EP contact on the underside of the package must be connected to V_{EE} . The two lines connecting the sense resistor to CSN and CSP must be routed as a differential pair directly from the resistor. A Kelvin connection is recommended. It is good practice to route the DIMO/DIMR, HS/HO, and LO/LS lines as differential pairs. The most important PCB board design consideration is minimizing the loop comprised by the main FET, synchronous FET, and their associated decoupling capacitor(s). Optimally this loop should be orthogonal to the ground plane.

APPLICATION INFORMATION

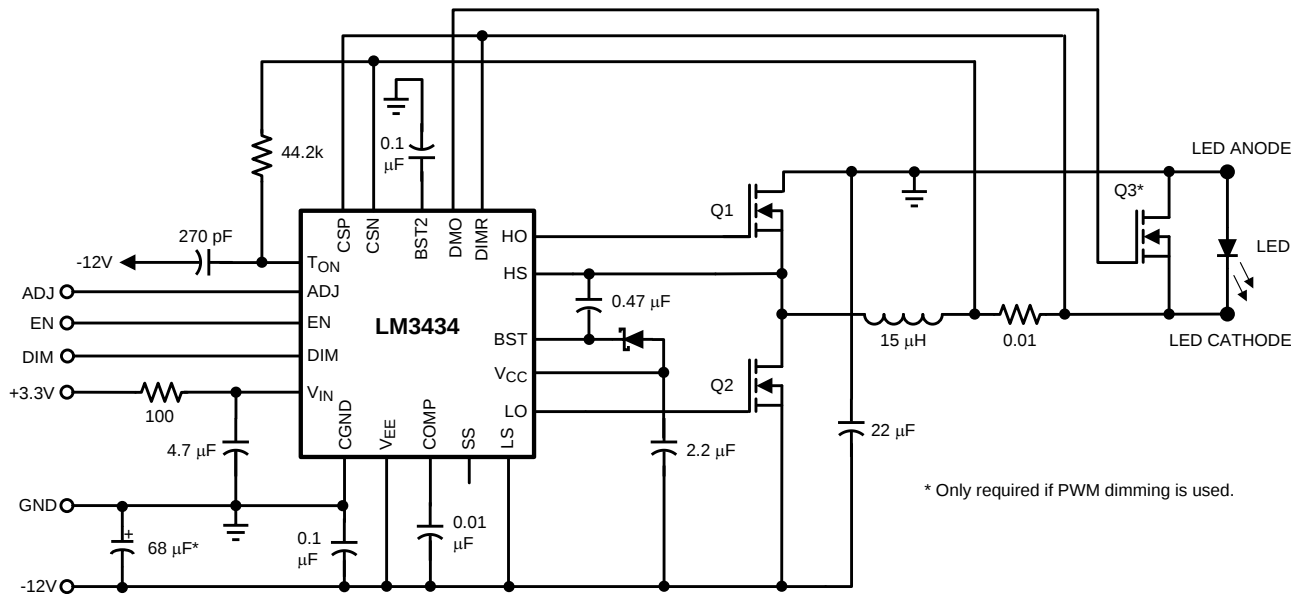


Figure 13. Up to 10A Output Application Circuit

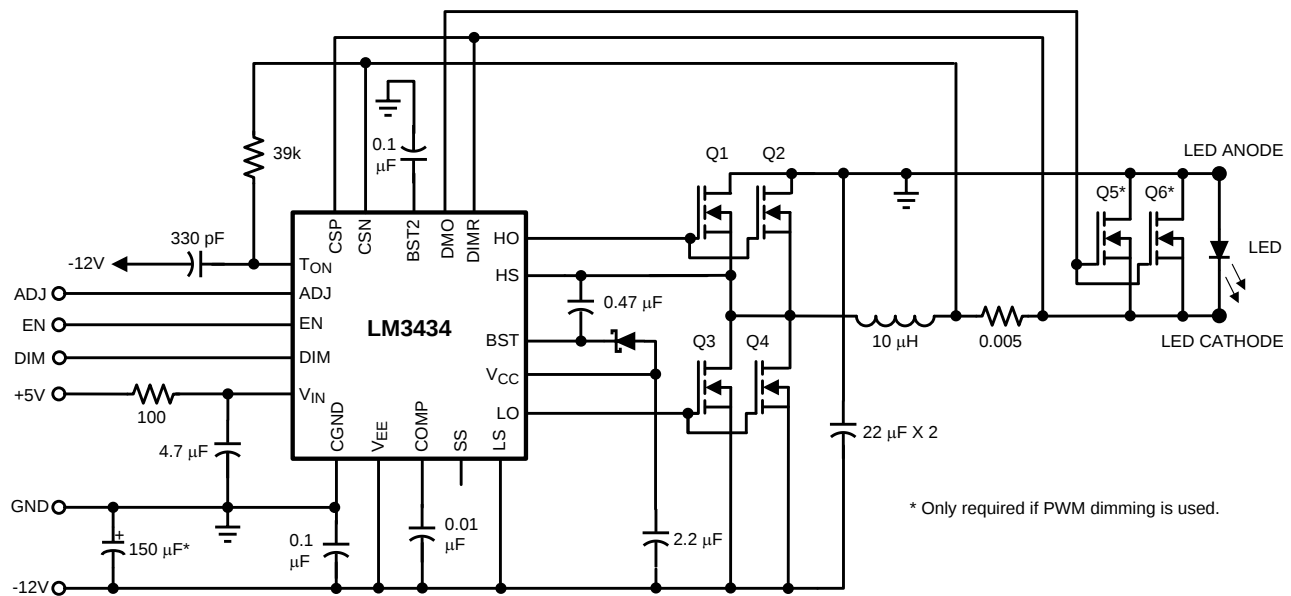


Figure 14. Up to 20A Output Application Circuit

Table 1. Some Recommended Inductors (Others May Be Used)

Manufacturer	Inductor	Contact Information
Coilcraft	GA3252-AL series, SER1360 series, and SER2900 series	www.coilcraft.com 800-322-2645
Coiltronics	HCLP2 series	www.coiltronics.com
Pulse	PB2020 series	www.pulseeng.com

Table 2. Some Recommended Input/Bypass Capacitors (Others May Be Used)

Manufacturer	Capacitor	Contact Information
Vishay Sprague	293D, 592D, and 595D series tantalum	www.vishay.com 407-324-4140
Taiyo Yuden	High capacitance MLCC ceramic	www.t-yuden.com 408-573-4150
Cornell Dubilier	ESRD series Polymer Aluminum Electrolytic SPV and AFK series V-chip series	www.cde.com
MuRata	High capacitance MLCC ceramic	www.murata.com

Table 3. Some Recommended MOSFETs (Others May Be Used)

Manufacturer	MOSFET	Contact Information
Siliconix	Si7386DP (Main FET, DIM FET) Si7668ADP (Synchronous FET) Si7790DP (Main FET, Synchronous FET, DIM FET)	www.vishay.com/company/brands/siliconix/
ON Semiconductor	NTMFS4841NHT1G (Main FET, Synchronous FET, DIM FET)	www.onsemi.com

REVISION HISTORY

Changes from Revision A (May 2013) to Revision B	Page
• Changed layout of National Data Sheet to TI format	14

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM3434SQ/NOPB	LIFEBUY	WQFN	RTW	24	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L3434	
LM3434SQX/NOPB	LIFEBUY	WQFN	RTW	24	4500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L3434	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

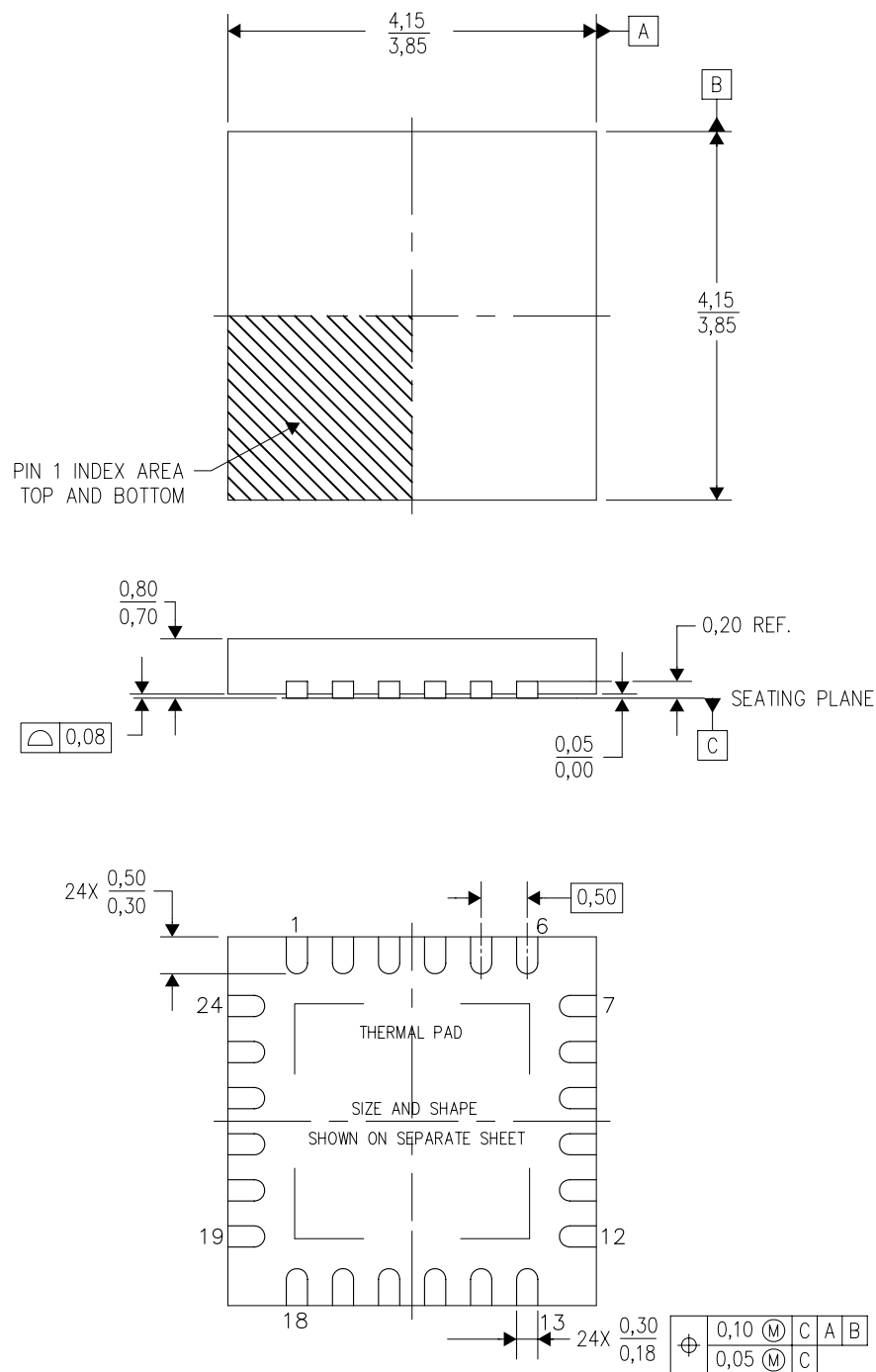
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

RTW (S-PWQFN-N24)

PLASTIC QUAD FLATPACK NO-LEAD



4206244/C 07/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Quad Flatpack, No-Leads (QFN) package configuration.
 - D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
 - E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
 - F. Falls within JEDEC MO-220.

IMPORTANT NOTICE

Texas Instruments Incorporated (TI) reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

TI's published terms of sale for semiconductor products (<http://www.ti.com/sc/docs/stdterms.htm>) apply to the sale of packaged integrated circuit products that TI has qualified and released to market. Additional terms may apply to the use or sale of other types of TI products and services.

Reproduction of significant portions of TI information in TI data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such reproduced documentation. Information of third parties may be subject to additional restrictions. Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyers and others who are developing systems that incorporate TI products (collectively, "Designers") understand and agree that Designers remain responsible for using their independent analysis, evaluation and judgment in designing their applications and that Designers have full and exclusive responsibility to assure the safety of Designers' applications and compliance of their applications (and of all TI products used in or for Designers' applications) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to their applications, Designer has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designer agrees that prior to using or distributing any applications that include TI products, Designer will thoroughly test such applications and the functionality of such TI products as used in such applications.

TI's provision of technical, application or other design advice, quality characterization, reliability data or other services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using TI Resources in any way, Designer (individually or, if Designer is acting on behalf of a company, Designer's company) agrees to use any particular TI Resource solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

Designer is authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNER AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Unless TI has explicitly designated an individual product as meeting the requirements of a particular industry standard (e.g., ISO/TS 16949 and ISO 26262), TI is not responsible for any failure to meet such industry standard requirements.

Where TI specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards and requirements. Using products in an application does not by itself establish any safety features in the application. Designers must ensure compliance with safety-related requirements and standards applicable to their applications. Designer may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers' own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.